Exploring Opportunities and Challenges of SRAM Based on 2D-Material FETs

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Two-dimensional transition metal dichalcogenides (2D TMDs) show promise for highly scaled logic transistors, leveraging their ultrathin profile and exceptional electrostatic control capabilities. Two-dimensional material (2DM)-based FETs have made significant strides in recent years, with advancements in wafer-scale monocrystalline growth, metal-2DM contact resistance, dielectrics, and back-end-of-line (BEOL) integration [1-3]. BEOL-compatible MOS transistors with a low thermal budget enable monolithic 3D (M3D) integrations for System-on-Chip (SoC) scaling. Potential channel materials exist for top-tier BEOL-compatible transistors, including two-dimensional materials, metal oxide semiconductors, carbon nanotubes, recrystallized Si, etc. [4-9]. Various device structures, including back-gated (BG), double gate (DG), and gate-all-around (GAA), are explored to enhance the driving capability of BEOL-compatible transistors.

In this presentation, I will discuss M3D SRAM cells with front-end-of-line (FEOL) Si FinFETs and BEOL 2DM FETs. I will discuss two M3D SRAM scenarios, including (1) $3DPG_{BEOL}$ and $3DPU_{BEOL}$ SRAM cells. The $3DPG_{BEOL}$ SRAM incorporates BEOL pass-gate (PG) nFETs combined with FEOL pull-down (PD) nFETs and pull-up (PU) pFETs. On the other hand, the $3DPU_{BEOL}$ considers BEOL PU pFETs combined with FEOL PD/PG nFETs. Through iterative electrical-thermal simulations [10], we demonstrate the on-current criteria ($I_{oncrit} = I_{onBEOL}/I_{onFEOL}$), defined as the I_{on} ratio of BEOL transistor to FEOL PD nFET for adequate read and write stability. A higher I_{oncrit} (89%) for $3DPG_{BEOL}$ SRAM is essential to mitigate read and write conflicts. In comparison to conventional 2D Si FinFET SRAM, the $3DPU_{BEOL}$ SRAM exhibits (a) a low I_{oncrit} (= 12.4%), (b) reduced cell area (-20.2%), (c) enhanced write stability (+70%), and (d) improved read (-15%) and write (-23%) speeds. Our results offer valuable insights into optimizing BEOL 2DM transistors for M3D integrations

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