Device, Materials, and Process Technologies Beyond the Exit of the Device Miniaturization Tunnel

H.-S. Philip Wong
Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA.
hspwong@stanford.edu

For the past fifty years, researchers of semiconductor technology have felt like walking inside a tunnel. There was a single path forward – two-dimensional down-scaling of device sizes, also referred to as 2D miniaturization. Other possible paths forward were quickly squashed by the steamroller of 2D miniaturization that provided exponential device density, higher power/energy efficiency, higher speed, and lower cost on a regular, predictable cadence. Technology advancement was synonymous with smaller feature sizes[1] and lithography was deemed the most important process step for advancing semiconductor technology. With device features approaching atomic scale, semiconductor technology has reached the exit of this tunnel. The future is bright at the exit of the tunnel as there are many possible paths[2] that create new opportunities for architectures that are extremely difficult (or even impossible) to implement using existing technology approaches that rely mainly on 2D miniaturization.

Many innovations across the entire system stack – from architectures to circuits, devices, fabrication processes, and materials – will provide large multiplicative benefits at the system level. While conventional wisdom optimizes for cost per transistor and economize on the use of transistors, future designs have additional optimization targets such as power/energy consumption, complexity of fabrication process/design/manufacturing and testing flows, cycle time for development and productization. These all have important implications for devices, materials, and process technologies of the future.

In this talk, I start with a top-down, application-driven perspective to ask: what are the future devices technologies? What kinds of materials and processes are needed to realize future generations of semiconductor technologies? How will the microelectronics ecosystem evolve in the future?

There are many paths forward for semiconductor technology advancement. Cost remains a key consideration for technology deployment. This is because lower cost enables ubiquitous deployment of the technology in society, and this means broad societal impact. To achieve higher performance, higher energy efficiency and more functionality for the integrated system, device technology needs to be application domain specific. This means system-technology co-design and end-to-end optimization will be key. Domain specificity demands the introduction of more materials and different device types into mainstream products and the process flow will become increasingly complex. Process technology development in the future must focus on reducing the cycle time.

All these will seed a change in the fabless-foundry ecosystem that has been in place for over 30 years. It is no longer possible to draw a clear boundary between design and fabrication. Lithography resolution will no longer be the main driver for technology advancement. Cycle time, both for the design and for the fabrication of chips, will have paramount importance.

Acknowledgements: This presentation was created in collaboration with Prof. Subhasish Mitra, Stanford University. This work is supported in part by Department of Defense Microelectronics Commons California-Pacific-Northwest AI Hardware Hub, Eccalon/DoD, National Science Foundation (award number 2235329), SRC JUMP 2.0 CHIMES Center and PRISM Center, member companies of the Stanford SystemX Alliance, Stanford Non-Volatile Memory Technology Research Initiative (NMTRI), and the Stanford Differentiated Access Memory (DAM) industry affiliate programs.

[1] S. Moore, "The node is nonsense," *IEEE Spectrum*, 2021.
[2] M. Liu, H.-S. P. Wong, "*How We'll Reach a 1 Trillion Transistor GPU*," *IEEE Spectrum*, March 28, 2024.